EE / CprE / SE 492 – sddec20-proj01

PROJECT TITLE: Machine learning for pilot biometrics

Week 9-10 Report

10/13/2020 – 10/26/2020 Client: Rockwell Collins Point of contact: JR Spidell Faculty Advisor: Akhilesh Tyagi

Team members:

Jianhang Liu--Data Manipulation SME
Feng Lin--Hardware SME
Xuewen Jiang --- Camera Interface SME
Xiuyuan Guo --- Algorithm SME
Sicheng Zeng - python SME
Junjie Chen --- C code SME
Sicheng Zeng - Team leader

Bi-weekly Summary

For these two weeks, we continue the work for the last two weeks such as improving the algorithm with various techniques like hyper-parameter tuning, quantization, pruning and hardware acceleration. PCB design hopes it will finish soon, and we will start the PCB layout review this week and hope we can start to order the materials.

Individual Contributions

Xuewen - Finish and update the bill of materials and get the total price of the daughter card. We decided to order 4 boards for the best cost performance. We did the layout review and hope that will finish soon.

Junjie Chen - This week we are writing on documentations for the various commands we had to use to set up the correct train and inference environment, different connectivity commands, things to watch for.

Feng Lin-figure out why the face-detection project can compile. Learning some simulating tools in order to observious ML layers' performance.

Sicheng Zeng- Using a new prune way to detect which method gets higher accuracy. I used a weight prune before. I try to use a dropout way on our project. I imported a sample on my computer, and it works great. I will work on pruning the model with less size and higher accuracy.

Xiuyuan Guo- During this time, changed our algorithm by changing the hyperparameter of our model model which include use the early stopping to find the best epoch and the learning rate scheduler to find the best learning rate.

Jianhang Liu- For the last week, Issac and I have made some changes based on the comments and questions on the layout review, and we will update and finalize the current PCB design in these weeks.

Team Member	Contribution	Hours Worked for the Week	Total Cumulative Hours
Junjie Chen	Rebuilt the DPU kernel with operation and architecture matching our project	8 h	83 + 8 = 41h
Sicheng Zeng	Work on using a new dropout pruning program to achieve higher accuracy	8h	54+10+9+8 = 89h
Xuewen Jiang	Finished BOM and ready to buy the materials, do layout reivew	5h	70h
Feng Lin	Documentation Vivado/Vitis software workflow.	6h	36h
Xiuyuan Guo	Change the hyperparameter of the given algorithm and use that to find the best so far to increase the accuracy and decrease latency of algorithm by reduce the layer of the CNN	10h	18+10=28
Jianhang Liu	Made some changes based on layout review, will update and finalize current PCB design recently	5h	70h

Pending Issues

Don't have experience on assemble PCB and testing Ran out virtual memory when building the DPU kernel

Plans

- 1. Optimize total latency about the pruned model running on board.
- 2. Increase after prune model accuracy
- 3. Increase swap space on host ubuntu machine to increase the RAM by swapping in between hard drive